AN-546
Application Note

E.FRIIS-MIKKELSEN
KROGSHØJVEJ 51 · 2880 BAGSVÆRD · TELEFON
DRENDSTRUPVEJ 74 · 8200 ÅRHUS N · TELEFON

SOLID-STATE LINEAR POWER AMPLIFIER DESIGN

Prepared by
Roy C. Hejhall
Applications Engineering

Linear amplifier design techniques and new RF power transistors developed specifically for HF (2-30 MHz) linear amplifier service are discussed.

MOTOROLA *Semiconductor Products Inc.*

© MOTOROLA INC., 1971

SOLID-STATE LINEAR POWER AMPLIFIER DESIGN

INTRODUCTION

Although most RF power amplifiers operate in the Class C* mode, a few applications require linear operation. The primary areas requiring linear amplification are suppressed carrier single sideband (SSB) and low level amplitude modulation (AM). The advantages of SSB over other modulation methods for high frequency communications have been widely discussed in other literature[1,2] and will not be repeated here.

A number of linear amplifier design techniques will be discussed in this note. Several parameters used to specify linear RF amplifier performance and methods for measuring these parameters will be explained. RF power transistors specifically designed for HF (2-30 MHz) linear amplifier operation will be discussed.

WHY LINEAR AMPLIFIERS?

The majority of RF power amplifiers in solid state transmitters are operated in a class C mode. Class C operation is widely used for CW, FM, AM, and pulsed transmitters for numerous reasons such as its high efficiency and zero no signal dissipation.

Class C amplifiers are inherently non-linear. However, in applications where only a single frequency signal is processed, the advantages of Class C operation outweigh the disadvantage of non-linearity.

When only a single frequency signal is being amplified, any non-linearity will generate only harmonics of that signal, regardless of the exponential order of the non-linearity. These harmonics can be filtered with passive L-C circuitry.

In the case of the multiple frequency signal, amplifier linearity becomes more important. The reason for this is that a multiple frequency signal makes it possible for non-linearities to generate spurious signals at frequencies which are very close to the frequency of the desired signal. These spurious signals cannot be conveniently attenuated by filtering.

The typical SSB RF signal consists of multiple frequencies with a bandwidth of about 3 kHz. In this case, the odd order exponential non-linearities generate spurious signals, which will be amplified and transmitted along with the desired SSB signal.

The problem is often illustrated by considering the case of a signal containing two frequencies, f_1 and f_2. A summary of some of the more troublesome spurious signals, which are generated by odd order non-linearities are given in Table 1.

TABLE I

Exponential Order of Non-linearity	Frequencies of Resulting Spurious Signals	Example: f_1 = 30.000 MHz, f_2 = 30.001 MHz
3rd	$2f_1-f_2$, $2f_2-f_1$	29.999 MHz, 30.002 MHz
5th	$3f_1-2f_2$, $3f_2-2f_1$	29.998 MHz, 30.003 MHz
7th	$4f_1-3f_2$, $4f_2-3f_1$	29.997 MHz, 30.004 MHz

The above listing contains only the spurious signals which are close to the desired frequencies f_1 and f_2 and therefore difficult to filter. The non-linearities will also generate the sum terms $2f_1 + f_2$, etc., but these like the harmonics of f_1 and f_2, are far removed in frequency.

It is beyond the scope of this report to show theoretically how the various spurious signals are generated. Rather the intent is simply to review the troublesome spurious signals and the non-linearities causing them. The interested reader is referred to Chapter 12 of Reference 1 for a theoretical treatment of spurious signal generation.

These spurious signals are not really a problem to a selective receiver tuned on channel. The problem lies in adjacent-channel interference which is the major reason for linearity requirements being placed on SSB transmitters.

Linearity Measurements

Before proceeding with the subject of linear amplifier design, a review of measurement conditions and techniques is in order.

These subjects will be covered to clarify the linearity data to be discussed later and to provide background information for those who may not be familiar with power-amplifier linearity measurements.

There are several methods that can be used to measure amplifier linearity. These include multiple tone (frequency) tests and noise tests.

Both methods consist of driving the amplifier under test with a complex signal. The nature of the test signal is such that distortion in the amplifier produces spurious outputs (called distortion products) which are very close in frequency to the desired signal and therefore not attenuated by the tuned circuits of the test amplifier.

*"Class C", as used in this report refers to operation with no signal conditions $I_C = 0$ and $V_{BE} = 0$, and a theoretical conduction angle of less than 180^o regardless of the actual conduction angle.

Circuit diagrams external to Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information in this Application Note has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

The amplitude of these distortion products at the amplifier output provides a convenient measurement of amplifier linearity. Such a method of specifying amplifier linearity is very practical. The measurement is feasible to perform and the results are in terms of what the entire linearity problem is all about – spurious signals.

All the linearity data in this report was measured using a two tone test signal with a frequency spacing of about 1 kHz between the test tones. The term "two tone test" is common in RF power literature, although it is somewhat misleading. The "tones" in this note refer to high frequency RF signals. Non-linear processing of such a signal produces distortion products in accordance with the listing in Table I. Linearity, or intermodulation distortion ratio (IMD), is then expressed as the ratio in decibels of one of the specified exponential order distortion products to one of the two desired tones. It is necessary that both input tones are of equal amplitude. When no exponential order is specified, it is understood that the reference is to the highest amplitude distortion product.

It is important to note carefully the conditions specified in the preceding paragraph for the distortion measurements performed in conjunction with this report. Some authors call out other ratios of distortion products to desired signals, and the designer should be sure of the measurement conditions before making distortion data comparisons.

The power level of a SSB signal (or any signal with a varying power level, such as an amplitude modulated signal) is usually specified in peak envelope power (PEP). The PEP of a signal is the average power level of the signal at the highest amplitude point of the signal envelope.

The multiple tone signal has a ratio of PEP to average power:

$$P_{average} = \frac{PEP}{N} \qquad (1)$$

where N = the number of tones. All the tones again have equal amplitudes.

Therefore, for the two tone test signals used in this report, a true average-reading power meter will indicate one half the PEP.

Sometimes more than two tones are used. The significant difference in testing with more tones is the reduction in average power for a given PEP as in equation 1. Therefore, a test involving three or more tones is a less stringent test from the standpoint of transistor dissipation and heating.

The noise, or "noise loading" type of linearity test has the advantage of not being limited to a discrete number of tones in the test signal. It basically consists of driving the test amplifier with a white noise signal containing a notch in its spectrum. Linearity is measured by noting the amplitude of noise in the notch at the amplifier output.

Linear Power Amplifier Transistors

The solid state linear power amplifier normally consists of one or more transistors and passive components.

Since a linear-passive component does not contribute to the distortion, the problem of linearity focuses on the distortion-producing element which is the transistor.

William Orr, who has done extensive work on vacuum tube linear amplifiers, has found that accurate linearity computations are extremely difficult due to the large number of variables involved. For example, amplifier linearity can vary significantly with changes of only a few percent in heater voltage, bias voltage, idling current, screen voltage, neutralization, grid and plate tuning and loading.[3]

The foregoing was included only to lend some insight into the difficulty of attempting a rigorous mathematical analysis of power amplifier linearity, since a similar set of difficulties exists with solid state linear amplifiers. Further, circuit parameters such as base RF input voltage may vary widely with the input and output tuning due to the very low input impedances and large collector-base feedback capacitances exhibited by transistors in the 10 to 100 watt class.

Probably the most significant transistor characteristic for linear amplifier operation is current gain linearity at high currents. A semiconductor manufacturer must take special care in designing a transistor for linear amplifier applications to make sure that h_{FE} does not drop at high collector currents. A transistor with rapid h_{FE} fall off at high collector currents will generally be a poor linear performer.

Besides beta linearity, other important transistor characteristics include proper design for a low and uniform operating junction temperature and the ability to survive mismatched loads.

Two RF power transistors which have been designed specifically for HF linear power amplifier applications are the 2N5941 and 2N5942. These devices are rated at 40 watts and 80 watts PEP output, respectively, at 30 MHz with IMD at -30 dB.

Somewhat greater power outputs can be realized at the expense of a lower IMD ratio, or improved IMD performance can be realized at reduced power output.

These figures compare favorably with those of vacuum tubes. Orr points out in his article that tubes have IMD's on the order of -25 dB at 70% to 100% of their maximum power levels, and that feedback is required to realize IMD's in the -30 to -40 dB range.

Figures 1-4 show the power output and linearity performance of 2N5941-2 transistors.

Linear Performance versus DC Supply Voltage

Operating a linear power amplifier transistor at reduced dc supply voltage drastically reduces the maximum power output for a given degree of linearity.

This is due to the problem of maintaining beta linearity at high currents. When the supply voltage is reduced, the transistor must deliver correspondingly higher collector current peaks for a given power output.

Typical performance data for the 2N5942 transistor illustrates this point. At 28 Vdc, the 2N5942 will deliver

Power Output and Linearity of the 2N5941 and 2N5942 Transistors

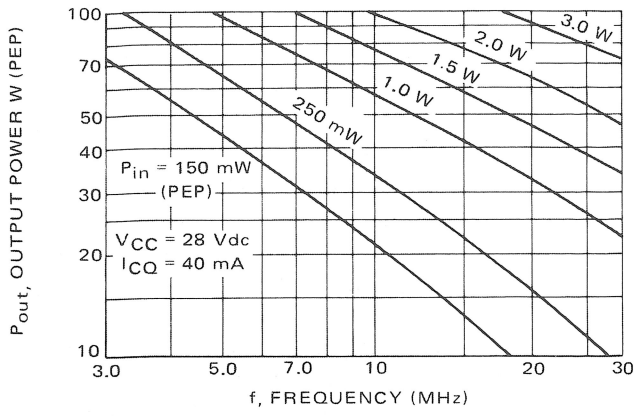


FIGURE 1 – 2N5942

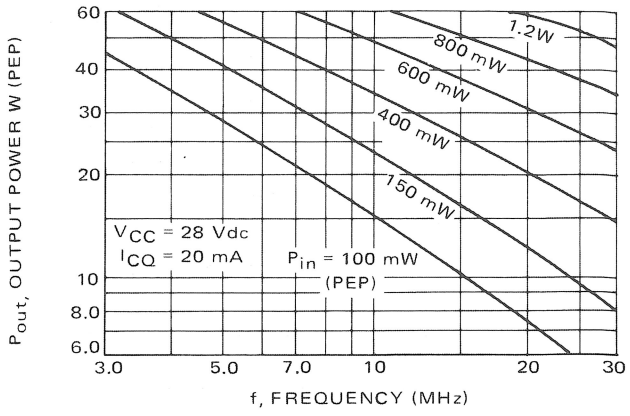


FIGURE 2 – 2N5941

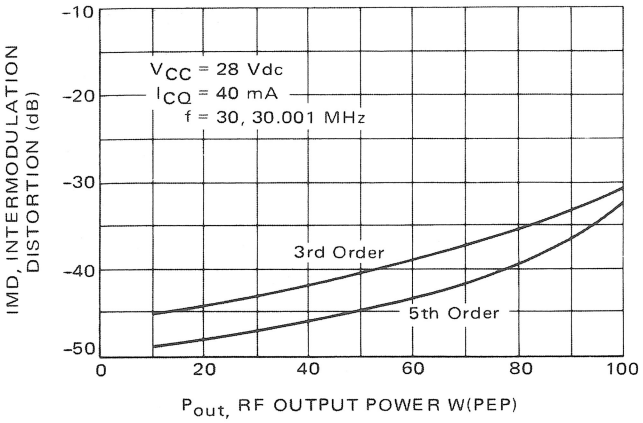


FIGURE 3 – 2N5942

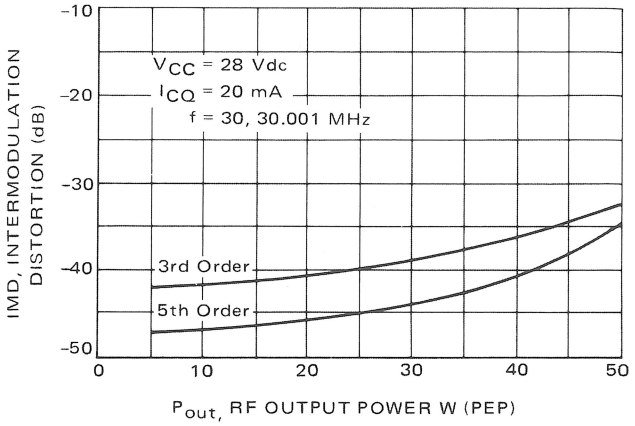


FIGURE 4 – 2N5941

typically 100 watts PEP output for an IMD ratio of -30 dB. The same transistor at 12.5 Vdc delivers typically 30 watts PEP for the same IMD ratio.

Thus, the 2N5941, which has only half the active chip area of the 2N5942, will deliver almost twice the linear power output at 28 Vdc (Figure 4) as the 2N5942 will deliver at 12.5 Vdc. The linear amplifier designer should therefore utilize the highest dc supply voltage he can (within the transistor ratings).

Linear Power Amplifier Design

Linear power amplifier design techniques center around two major areas – dc bias and impedance matching.

Impedance matching will be discussed in general first and followed by a discussion on biasing for linear operation.

The impedance matching problem is similar to that of the Class C amplifier except that linearity places more restrictions on the transistor collector load impedance. See Reference 4 for a general discussion of RF power amplifier network design.

Neither the input RF matching network configuration or input tuning significantly affects linearity. Therefore, the designer is free to concentrate on the major problem at hand for the input network – getting the RF drive power into the very low impedance transistor. For broadband power amplifiers, this is difficult.

The linear amplifier output network must present the collector with the proper complex load impedance. Output network design as well as output tuning is somewhat more critical than in the case of the Class C amplifier, as linearity is affected by collector load impedance.

Of particular importance in output network design is the correct power level to use in the network calculations.

Average power output varies widely depending on the nature of an SSB signal (single tone, multiple tone, voice, etc.). Linear amplifier design is based on a particular value of peak envelope power, not average power. Average power has no real bearing on the design, except for thermal considerations.

The complex collector load impedance should be the conjugate of the transistor parallel output capacitance and the parallel load resistance, R_L', computed from the expression:

$$R_L' = \frac{(V_{CC})^2}{2P} \qquad (2)$$

2N5942 Large Signal Impedance Data

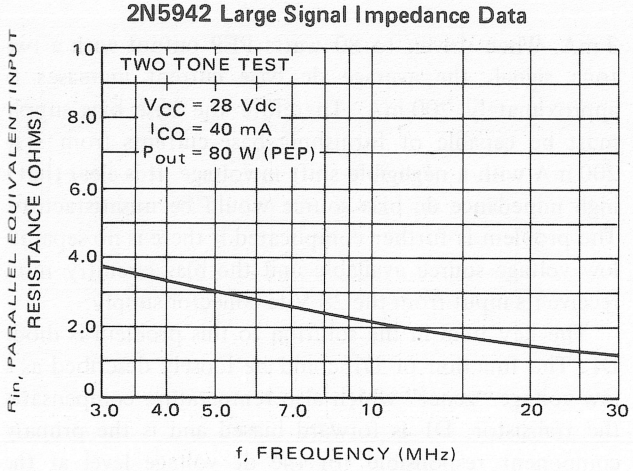


FIGURE 5 – 2N5942

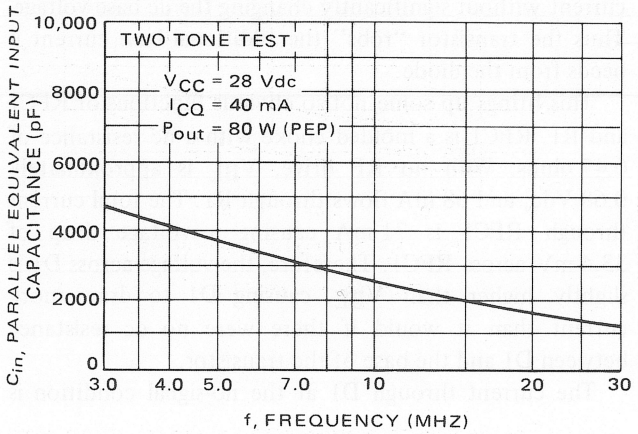


FIGURE 6 – 2N5942

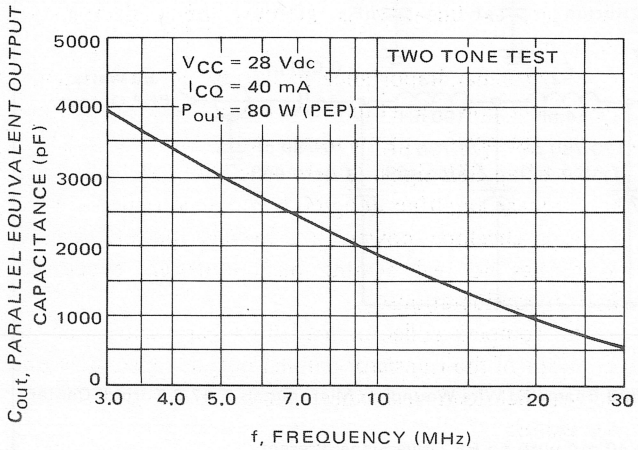


FIGURE 7 – 2N5942

where V_{CC} = dc collector supply voltage
P = RF power output

In the case of the linear amplifier, the desired value of peak envelope power is used in equation 2 to compute the load resistance. Thus the collector load impedance ideally should be the conjugate of R_L' in parallel with C_{out}.

Figures 5-7 show the large-signal impedances for the 2N5942 when operating in a linear amplifier circuit.

The bias network design for linear power amplifiers is critical and completely different from the Class C amplifier zero bias situation.

The typical Class C amplifier is operated with both the base and emitter connected to dc ground. Thus, the transistor is completely "off" when no driving signal is present.

The linearity of a solid state power amplifier may be greatly improved by operation with forward bias. "Forward bias" refers to operation with a finite no signal collector current.

The extreme case of forward bias is, of course, Class A operation. Class A operation provides the greatest linearity at an extreme sacrifice in efficiency.

As power output is increased, practical transistor dissipation limitations dictate Class B operation. Class B linear amplifiers with power outputs up to 80 watts PEP are described in this report.

Optimum no-signal collector currents for 10-100 watt transistors are in the 5-50 mA range.

Class B bias circuit design is complicated by thermal runaway problems and large variations in power-amplifier transistor base current as RF drive level is varied.

For best linearity, the dc base voltage should remain constant as the RF drive level is varied. This situation is in conflict with the conditions required to prevent thermal runaway.

Some rather exotic schemes with multi-stage dc amplifiers have been developed for linear power amplifier biasing, and such schemes are limited only by the designer's imagination. It is also possible to achieve excellent results without the use of gain elements in the bias circuitry. All the linear amplifiers described in this report use only a diode and passive components in the bias circuitry.

Details of the individual bias circuit designs will be covered in the circuit descriptions to follow.

80 Watt Linear Amplifier

Figure 8 shows a 30 MHz linear amplifier using a 2N5942 transistor. This amplifier will deliver 80 watts PEP output with the following typical performance:

Power gain = 13 dB
Intermodulation distortion ratio = -34 dB
Collector efficiency = 40%
DC supply voltage = 28 Vdc

This amplifier was designed to see what performance could be obtained at a single frequency with completely flexible wide range impedance matching networks.

The output network is a double pi designed for 80 watts PEP.

The input network uses a center-tapped transformer. The basis for the design is the 2N5942 large-signal input impedance (Figure 5 and 6). The circuit does provide an excellent match to a 50 ohm driving source.

There is more than is readily apparent to the dc bias network. The emitter is dc grounded, with a dc forward bias voltage applied to the base through RFC1. The bias network is fed from the 28 Vdc collector supply.

The Class B bias network should meet several requirements. It must:

1) Permit the transistor to operate with a no-signal collector current to meet an IMD requirement with reasonable collector efficiency.

2) Provide bias conditions which yield reasonable IMD over the full dynamic range of the amplifier.

3) Prevent thermal runaway.

The bias network in this amplifier has some unique features to meet the above requirements without using gain elements.

Requirement 1 is best met by not permitting the dc base voltage to change more than about 0.1 Vdc as the RF drive level is varied from zero to full power.

Requirement 2 is best met by increasing the no-signal collector current. A no-signal collector current of 40 mA was selected as a good compromise value for the 2N5942. This will be discussed in more detail later.

Requirement 3 calls for some means of reducing base voltage with increasing temperature.

The need to maintain an almost constant base voltage calls for a low dc source impedance system. The reason for this lies in the transistor base currents.

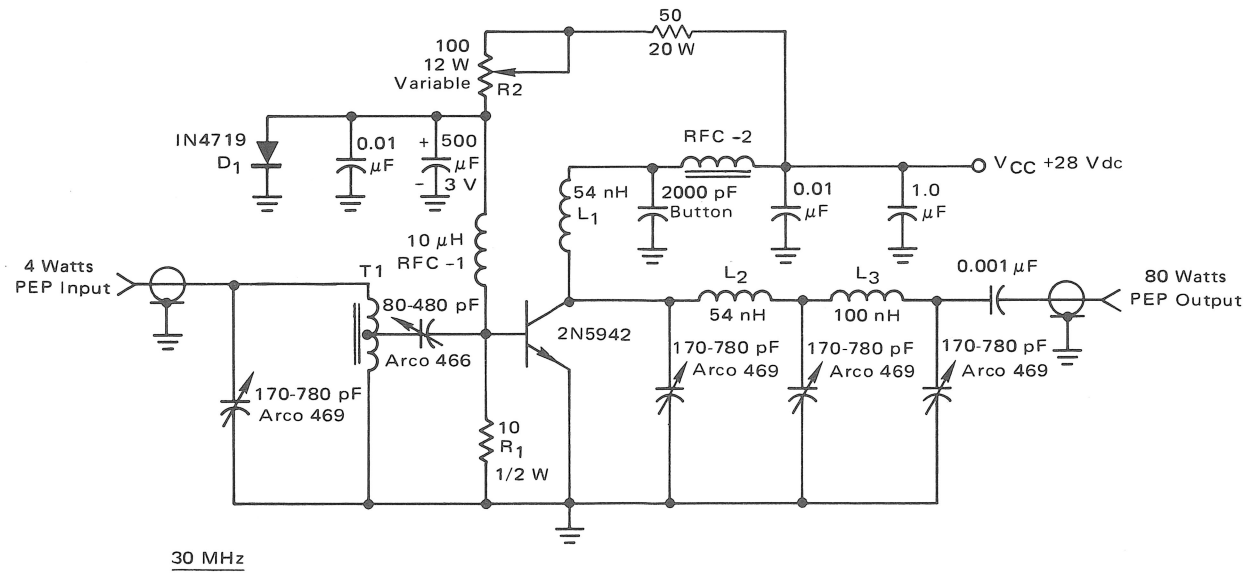
With zero RF drive, the 2N5942 base current is about 3 mA. When driven to 80 watts PEP output with a two tone signal, the average dc base current increases to approximately 200 mA. Therefore the base bias supply must be capable of furnishing base currents from 3 to 200 mA with a negligible shift in voltage. It is clear that a high impedance dc bias source would be unsatisfactory. The problem is further complicated if there is no separate low voltage source available and the bias circuitry must receive its input from the 28 Vdc collector supply.

The key item in the solution to this problem is diode D1. The function of D1 could be loosely described as a low voltage "zener" which also temperature compensates the transistor. D1 is forward biased and is the primary component responsible for the dc voltage level at the transistor base. D1 is thermally coupled to the transistor by mounting it on the same heat sink and therefore provides temperature compensation due to its decrease in forward voltage with increasing temperature.

When RF drive is applied, the transistor receives its additional base current by diverting current from the diode D1. The diode can provide this additional base current without significantly changing the dc base voltage. Thus the transistor "robs" the additional base current it needs from the diode.

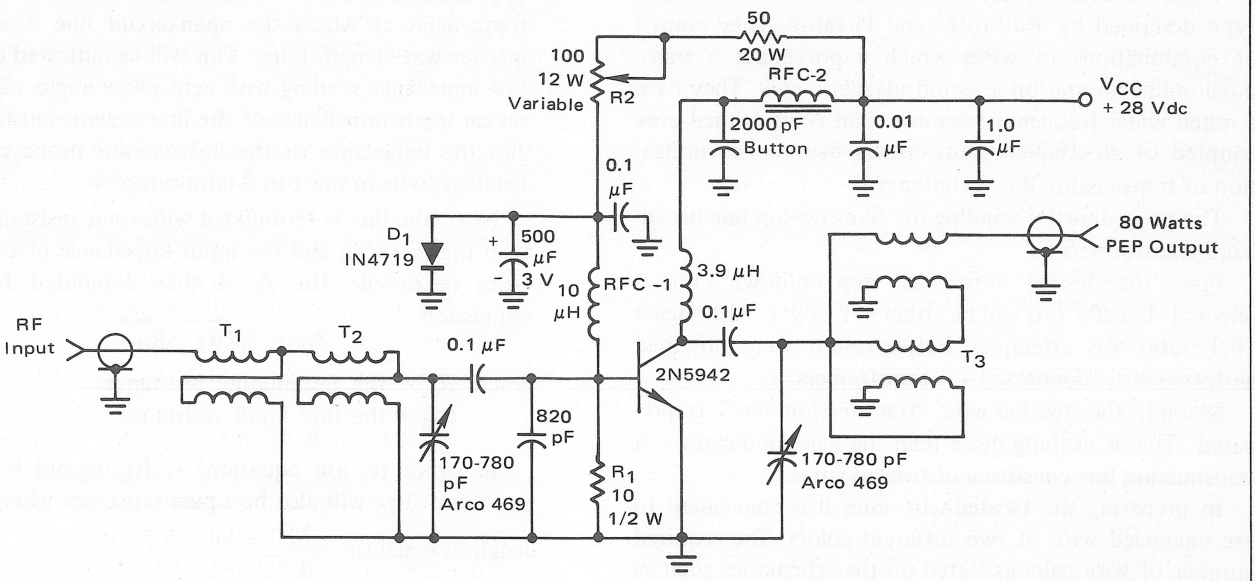
This brings up some not so obvious functions of RFC1 and R1. RFC1 is a molded choke with a dc resistance of 0.47 ohms. With no RF drive, V_{BE} is approximately 0.68 Vdc, and 68 mA flows through R1. The total current through RFC1 is 71 mA causing a voltage drop of 33.4 mV across RFC1. Therefore, the voltage across D1 is slightly higher than V_{BE}, causing D1 to draw more current than it would if there were no dc resistance between D1 and the base of the transistor.

The current through D1 at the no-signal condition is



L_1, L_2 = 2 1/2 Turns #14 AWG, 1/4" I.D., 3/8" L.
L_3 = 4 1/2 Turns #14 AWG, 1/4" I.D., 1/2" L.
RFC -2 = Ferroxcube - VK200 19/4B Ferrite Choke
T_1 = 20 Turns of #20 Enameled Wire Wound on Micrometals T 47-6 Toroid. Center Tapped
Adjust R_2 for I_C = 40 mA with no RF Drive Signal Present.

FIGURE 8 – 80 Watt PEP Linear Amplifier



T_1: 4:1 6 Turns of 2 Twisted Pairs of #26 AWG Enameled Wire (6 Crest Per Inch) Wound on Stackpole 57-9322 #11 Toroid.
T_2: 4:1 4 Turns of 4 Twisted Pairs of #26 AWG Enameled Wire (6 Crest Per Inch) Wound on Stackpole 57-9322 #11 Toroid.
T_3: 1:9 10 Turns of 3 Twisted Pairs of #28 AWG Enameled Wire (8 Crest Per Inch) Wound on Two Stackpole 579074 #11 Toroid
Adjust R2 for I_C = 40 mA with no RF Drive Signal Present
RFC – 2 = Ferroxcube V K200 19/4B Ferrite Choke

FIGURE 9 – 80 Watt 2-30 MHz Broad Band Linear Amplifier

about 260 mA, and this is the source of the increased transistor dc base current at full power.

If there were no dc resistance between D1 and the base of the transistor, the no-signal current through D1 would be only about 120 mA. Under these conditions, the transistor would steal all of the diode current at full power. D1 then would shut off and the additional base current could only come from the bias source (which approximates a constant-current source) by reducing the current through R1 as the base voltage shifts downward. The net result of all this would be a dc base voltage shift of more than 0.5 V from zero to full power, which would severely degrade the amplifier linearity.

There is an additional benefit derived from the base circuit operation. The reduction of D1 current with RF drive level results in additional temperature compensation beyond the simple reduction of diode drop with temperature. The voltage across D1 drops with RF drive level for two reasons – the heating of D1 and a reduction in D1 current.

This results in excellent temperature compensation, and the amplifier has absolutely no tendencies toward thermal runaway at full power with heat sink temperatures in excess of 110°C.

Resistor R1 has a dual function. First, it causes current flow through RFC1 when no RF driving signal is present. This is the key to the difference in voltage between the anode of D1 and the 2N5942 base. Second, R1 reduces the total RF impedance from base to ground and thereby improves the stability of the amplifier.

As stated in biasing requirement 2, maintaining linearity in an amplifier over the entire dynamic range of the amplifier presents a biasing problem.

At practical levels of quiescent collector currents, in Class B amplifiers, IMD generally degrades at low-power output levels. Thus, a typical plot of the IMD ratio for an amplifier may show -30 dB at full power, -35 dB at half power, -31 dB at one-tenth power, rising to perhaps -25 dB at less than one-tenth power.

About the only solution to low distortion at low power for a power amplifier is to increase the quiescent collector bias current. However, if one wishes to prevent the IMD ratio from ever being worse than it is at full power, bias currents approaching Class A operation may be required.

A practical solution can be achieved by considering the absolute magnitude of the distortion products, and insuring that they remain below their full-power output levels.

For example, if an amplifier which has an IMD ratio of -30 dB at full power exhibits an IMD ratio of -25 dB when the power output is reduced by 15 dB, the distortion products are still 10 dB below what they were at full-power output. This is despite the fact that the IMD ratio has degraded.

The criterion for low-power IMD used in the design of the amplifiers described in this report is that the full power IMD ratio rating shall be maintained for all power output levels from full power output down to 10 dB below full power.

80 Watt Broadband Linear Amplifier

Figure 9 shows a 2-30 MHz broadband 80 watt PEP linear amplifier. The bias circuit is identical to the 80 watt linear amplifier first described. The key to broadband operation of this second amplifier lies with transformers T_1, T_2, and T_3.

These transformers are the transmission-line broadband type described by Ruthroff[5] and Pitzalis[6]. They consist of combinations of wires which approximate a transmission-line wound on a toroid magnetic core. They have a much wider frequency response than conventional core coupled or air-coupled transformers due to the utilization of transmission-line techniques.

The procedure for winding the transmission-line broadband transformers is:

First, the desired impedance step up/down ratio is selected. Usually this will be either 4:1 or 9:1. Although a 16:1 ratio was attempted better results were obtained with two series connected 4:1 transformers.

Second, the twisted-wire "transmission line" is prepared. This is nothing more than the name indicates – a transmission line consisting of twisted wires.

In preparing the twisted-wire lines it is convenient to use enameled wire of two different colors. The required number of wire pairs as stated on the schematics such as "three twisted pairs", means 3 wires of each color are then twisted to achieve the required number of crests per inch. A drill motor makes a convenient "wire twister". A single "crest" is formed by all the wires of one color.

The key parameters for the transmission line are characteristic impedance (Z_O) and length. These parameters are optimized for transformer bandwidth.

The optimum characteristic impedance of the twisted wires of a transmission line transformer is given by the following expression:

$$Z_O = \sqrt{R_1 \, R_2} \qquad (3)$$

where R1 and R2 are the two impedances to be matched.

The optimum length is somewhat shorter than an eighth wave-length at the highest frequency of operation.

The variables affecting Z_O include wire size, tightness of the "twist" which can be designated in crests per inch, and number of wires.

In general, the Z_O may be decreased by using larger wire, a tighter twist (more crests per inch), or increasing the number of wires.

The Z_O of the twisted wire lines may be measured prior to winding the lines on the cores. Any convenient method of measuring Z_O may be employed, depending on the equipment available.

The twisted wire line Z_O measurements for the amplifiers described in this report were made with a Hewlett-Packard model 4815A Vector Impedance meter. Two measurement techniques were investigated.

The first method involved input impedance measurements on a quarter wave length ($\frac{\lambda}{4}$) of line. The procedure was as follows:

Solder together all of the wires of one color at one end of a 2 to 3 foot length of the twisted line. Repeat for the other colored wires on the same end of the line. Do the same at the other end of the line. Connect the two bundles at one end of the line to the two terminals of the impedance meter, leaving the two groups of wires on the opposite end of the line unconnected. Then determine the frequencies at which the open-circuit line is exactly a quarter wave-length long. This will be indicated by a very low impedance reading with zero phase angle. The theoretical input impedance of the line is zero, but line losses and the impedance of the instrument's probe cause the readings to be in the 1 to 2 ohm category.

Next, the line is terminated with some resistance other than the line's Z_O and the input impedance of the line is again measured. The Z_O is then computed from the expression

$$Z_O = \sqrt{R_L \cdot R_{in}} \qquad (4)$$

where R_L = the terminating resistance
R_{in} = the line input resistance

In order to use equation 4, R_L should be a pure resistance. R_{in} will also be a pure resistance when the line length is equal to $\frac{\lambda}{4}$.

The second method consists of making input impedance measurements on a section of line at a frequency where the line length is less than $\frac{\lambda}{4}$ with first an open circuit and then a short circuit termination. Under these conditions, the line input impedance will be a pure reactance, and Z_O may be computed from the expression:

$$Z_O = \sqrt{|X_S| \cdot |X_O|} \qquad (5)$$

where

X_S = the input reactance of the line with a short circuit termination

X_O = the input reactance of the line with an open circuit termination

Of these methods, the first yielded better results.

As a final step with either method, the computed Z_O was verified by terminating the line with a load equal to Z_O and measuring the line input impedance over a decade of frequency. With the correct termination the input impedance of the line will of course be equal to Z_O and constant over a large frequency range.

Then the required number of turns are wound on the magnetic core.

The cores selected for the transformers of this amplifier are of ferrite material usually used at frequencies below 10 MHz. Optimum performance over the HF range was achieved with a lower frequency core, since these transformers are not core coupled and the primary function of the core is to increase winding inductances to improve performance at the lower end of the operating frequency range.

Finally, as described in the section on measurement of the characteristic impedance of the line, all the wire ends of the same color at each end of the winding, are connected together, thus forming a two-conductor winding as shown in Figure 10. The transformer is then connected into the amplifier as shown in the schematic diagrams.

This completes the single-core transformer. In the case of a multiple-core unit such as the 9:1 transformer, the

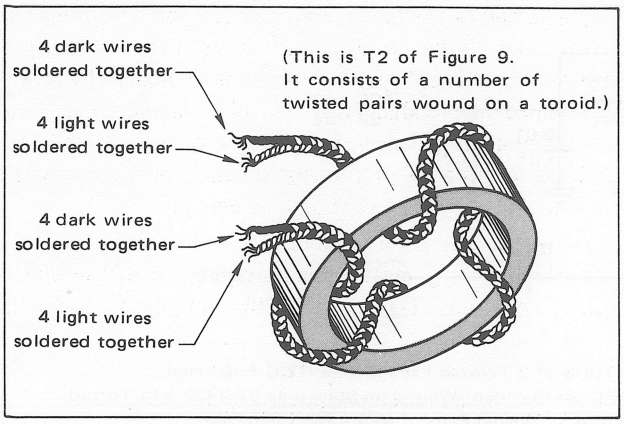


FIGURE 10 – Broadband Transformer of Transmission–line Type.

two cores are prepared separately and then wired together in the manner shown in the schematic diagram.

For a more detailed discussion of these transformers, see References 5 and 6.

Returning specifically to the circuit of Figure 9, the performance specifications and design features will be discussed.

T1 and T2 are series connected 4:1 transformers for a theoretical step down of 16 to 1 for the base. Note that T2 is wound differently from T1 since it is transforming lower inpedance levels.

The optimum characteristic impedance for T1 and T2 are computed as 25 and 6.25 ohms, respectively.

An impedance of 25 ohms can be readily achieved in practice, but 6.25 ohms is more difficult. The actual characteristic impedance achieved with T2 was 8 ohms.

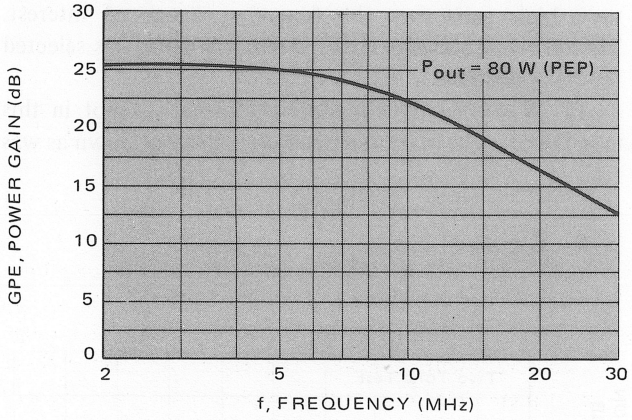


FIGURE 11 – Power Gain Versus Frequency Performance of Amplifier Shown in Figure 9

The optimum characteristic impedance for output transformer T3 is 16.7 ohms. This value was achieved.

Figure 11 shows a plot of power gain versus frequency for 80 watts PEP output power. The typical collector efficiency at 30 MHz with 80 watts PEP output is 43% for this amplifier.

The amplifier was mismatch tested at 80 watts PEP with a two tone test signal by subjecting it to an infinite VSWR load at all phase angles. The 2N5942 transistor was not damaged.

Network design for broadband linear amplifiers is further complicated by linearity considerations.

The critical area is the amplifier output network, since the complex collector load impedance has a significant effect on linearity. Therefore, a network which provides a satisfactory load from a gain standpoint may still present difficulties in achieving optimum linearity performance.

The networks of this amplifier achieved a decade of bandwidth at the expense of some linearity performance.

At 80 watts PEP output, the IMD ratio at 30 MHz is typically -32 dB, while at some lower frequencies the IMD is slightly worse at -25 to -30 dB.

Figure 12 is a plot of IMD versus power output at 4, 15, and 30 MHz. IMD performance of -30 dB can be achieved over the entire operating frequency range of the amplifier, if power output is limited to 70 watts PEP.

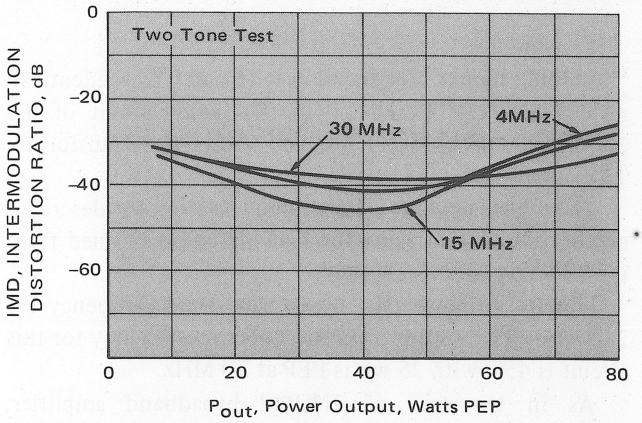


FIGURE 12 – IMD vs Power Output of Amplifier shown in Figure 9

Note that feedback has not been used and that no attempt has been made to make the gain of this amplifier flat with frequency.

The objective here was to design an amplifier which would utilize the useful gain of the 2N5942 over greater than a decade of frequency with no tuning. That this has been accomplished reasonably well can be demonstrated by comparing Figure 11 with the gain versus frequency characteristics of the 2N5942 transistor (Figure 1).

A broadband transmitter utilizing such an amplifier would include a gain control.

An example of a broadband amplifier at a lower power level utilizing feedback to achieve a constant gain versus frequency characteristic is given later in this report.

25 Watt Broadband Linear Amplifier

Figure 13 shows a 2-50 MHz broadband 25 watt PEP linear amplifier using the 2N5070 transistor.

Again the key components in this amplifier are the broadband transformers T1, T2, and T3, all of which are a 4:1 ratio.

This amplifier also illustrates the practicality of developing a number of standard broadband transformer

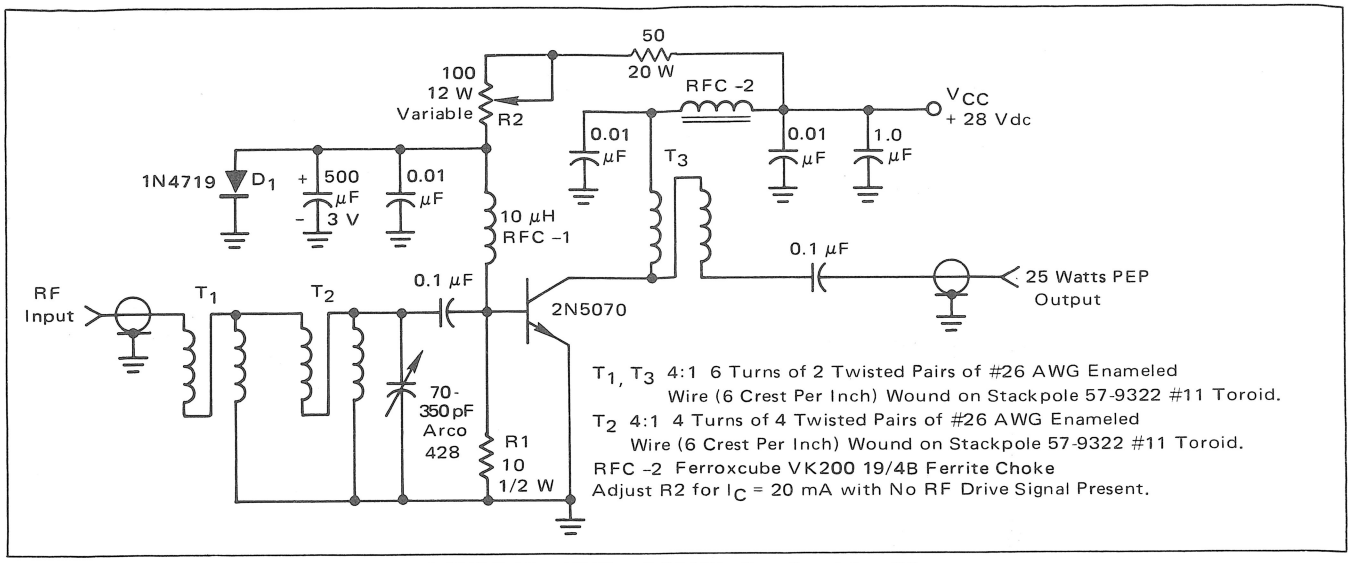


FIGURE 13 – 25 Watt 2-50 MHz Broadband Amplifier

"building blocks" for general use. T1 and T2 are identical, respectively to T1 and T2 in the input circuit of the 2N5942 amplifier just described. And output transformer T3 is identical to T1.

The bias network is the same as the one described earlier. Note that again the bias voltage is obtained from the 28 Vdc collector supply.

Figure 14 shows the power gain versus frequency for 25 watts PEP output. Typical collector efficiency for this circuit is 45% with 25 watts PEP at 30 MHz.

As in the case of 2N5942 broadband amplifier, feedback was not employed. The amplifier therefore has a gain versus frequency characteristic which approximates that of the transistor over the frequency range of 2 to 50 MHz.

Figure 15 shows the IMD ratio of the amplifier as a function of output power at 4.0, 15.0, and 30 MHz.

Class A Linear Amplifier with Feedback

Figure 16 shows a low level broadband linear amplifier of the type which might be used in the pre-driver stages of a HF SSB transmitter. This amplifier utilizes Class A bias for excellent linearity and negative feedback for minimum gain dependence on frequency. It delivers 0.2 watts PEP output from 0.5 to 50 MHz with a gain flatness of ±1 dB with a -35 dB IMD ratio. Since it is a Class A amplifier, linearity improves at lower power outputs.

In order to utilize the negative feedback required for constant gain over two decades of frequency and still achieve useful gain, it is desirable to have a transistor with very high gain over the frequency range of interest. Therefore, a 2N3866 UHF power transistor was selected for this amplifier.

T1 is another broadband transformer, except in this case the 50 ohm load is stepped up instead of down as was

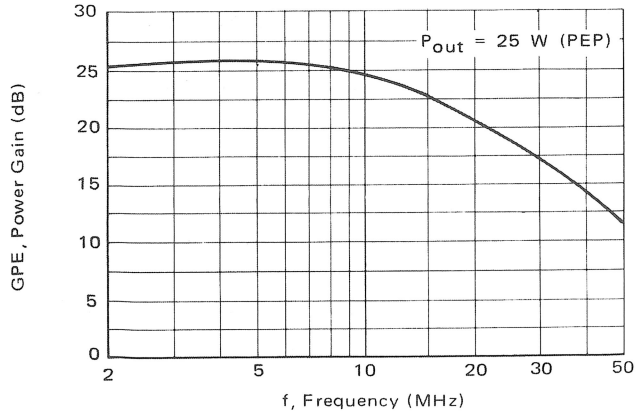


FIGURE 14 – Power Gain Versus Frequency Performance of Amplifier Shown in Figure 13

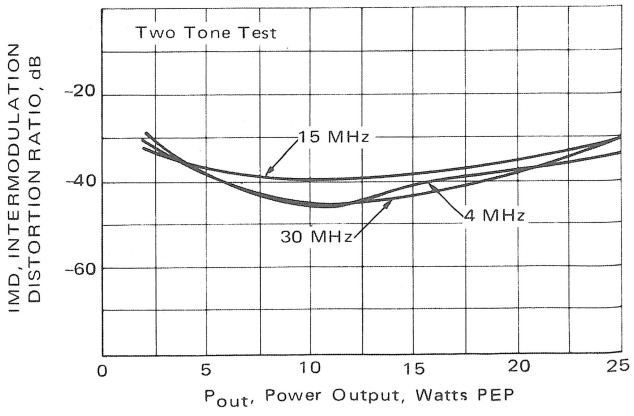
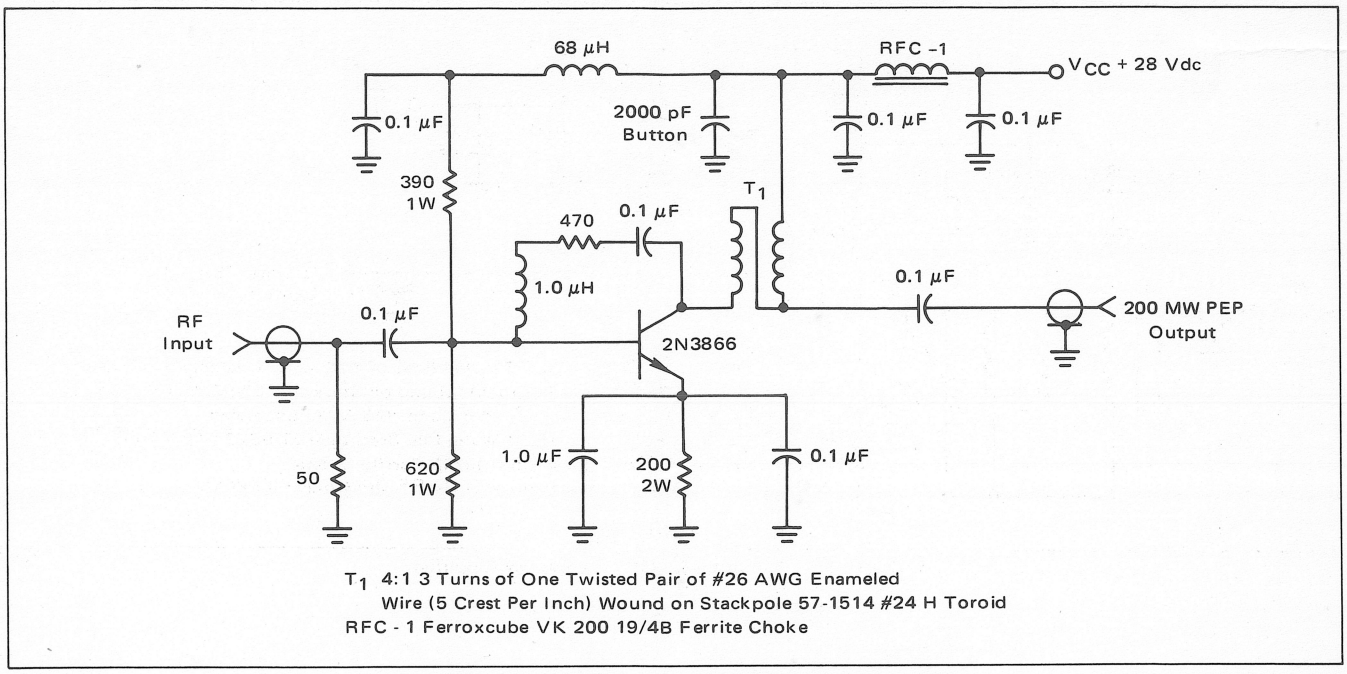


FIGURE 15 – IMD versus Power Output of Amplifier Shown in Figure 13.



T_1 4:1 3 Turns of One Twisted Pair of #26 AWG Enameled Wire (5 Crest Per Inch) Wound on Stackpole 57-1514 #24 H Toroid

RFC - 1 Ferroxcube VK 200 19/4B Ferrite Choke

FIGURE 16 – 200 mW .5-50 MHz Class A Linear Amplifier

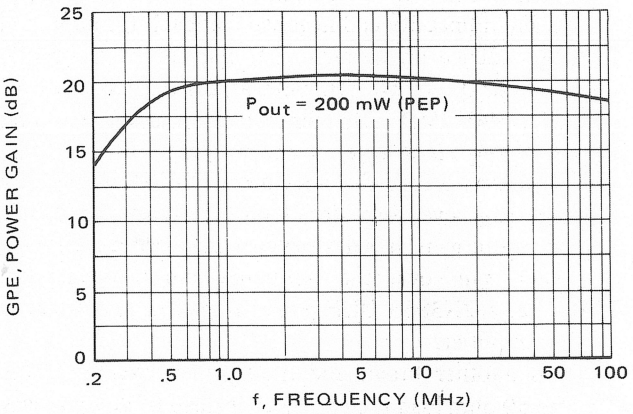


FIGURE 17 – Power Gain versus Frequency Performance of Amplifier Shown in Figure 16.

done with higher power amplifiers described in this note.

One should note that the feedback network between collector and base is designed to provide greater negative feedback at the lower frequencies.

Figure 17 shows the gain versus frequency performance of the amplifier with 200 mW PEP output.

Summary

Both Class A and Class B linear power amplifiers with and without feedback have been described.

The key to amplifier linearity is operation with forward bias (Class A or B).

The most important amplifier design considerations for linearity are the dc bias system and proper collector load impedance.

Acknowledgments:

The author wishes to acknowledge the following contributors to this work.

Brent Trout designed the amplifier shown in Figure 16.

Edward Loupe constructed the amplifiers, performed all the complex measurements, and provided many excellent suggestions both on the amplifier designs and the preparation of this report.

References:

1) Pappenfus, Bruene, and Schoenike, "Single Sideband Principles and Circuits", McGraw-Hill.

2) Honey and Weaver, "An Introduction to Single Sideband Communications," Proc. IRE, Vol. 44, No. 12, December 1956.

3) Orr, "Intermodulation Distortion in Vacuum Tubes", Single Sideband for the Radio Amateur, 1970 Edition, American Radio Relay League.

4) "Systemizing RF Power Amplifier Design", Motorola, Inc., Application Note An-282.

5) Ruthroff, "Some Broadband Transformers", Proc. IRE, Vol. 47, No. 8, August, 1959.

6) Pitzalis, "Broadband Transformer Design for RF Transistor Power Amplifiers", paper presented at the 1968 Electronics Components Conference.

7) Pitzalis, Horn and Baranello "Broadband 60-W HF Linear Amplifier" IEEE Journal of Solid State Circuits Vol. SC-6 No. 3, June 1971.

MOTOROLA Semiconductor Products Inc.